

IN THE CLAIMS:

1 1 (presently amended). A semiconductor device comprising:
2 a thyristor having thyristor body regions including first and second immediately
3 adjacent base regions between first and second emitter regions;
4 a first control port configured and arranged to capacitively couple a first signal at least
5 to the first base region; and
6 a second control port configured and arranged for receiving a second signal generated
7 outside of the thyristor and for coupling [[a]] the second signal at least to the second base
8 region, the second signal being adapted to control holding current or forward blocking voltage
9 of the thyristor as a function of temperature.

1 2 (original). The semiconductor device of claim 1, further comprising:
2 a circuit arrangement electrically coupled to the second control port and configured and
3 arranged to apply the second signal to the second control port.

1 3 (original). The semiconductor device of claim 2, wherein the circuit arrangement includes
2 a temperature sensing circuit electrically coupled to the thyristor and configured and arranged
3 to apply the second signal to the second control port as a function of the temperature of the
4 thyristor.

1 4 (original). The semiconductor device of claim 2, wherein the second signal applied by the
2 temperature sensing circuit is adapted to increase bipolar gains of the thyristor when the
3 temperature of the thyristor is below a selected threshold.

1 5 (original). The semiconductor device of claim 4, wherein the selected threshold is a
2 temperature at which the holding current of the thyristor would exceed a design holding
3 current value.

1 6 (presently amended). A memory device comprising:

2 at least one thyristor having thyristor body regions including first and second
3 immediately adjacent base regions respectively coupled to and between first and second
4 emitter regions;

5 a first control port configured and arranged to capacitively couple a first signal at least
6 to the first base region;

7 a first circuit configured and arranged to detect a temperature-related failure of the
8 thyristor to maintain its conductance state during a standby mode or to maintain its blocking
9 state; and

10 a second circuit including a second control port configured and arranged for receiving a
11 second signal generated outside of the thyristor and for coupling [[a]] the second signal at least
12 to the second base region as a function of the detected failure for controlling holding current or
13 forward blocking voltage of the thyristor.

1 7 (original). The memory device of claim 6, further comprising a reference thyristor, the
2 first circuit being configured and arranged to detect the failure condition from the reference
3 thyristor.

1 8 (original). The memory device of claim 7, wherein the reference thyristor is configured
2 and arranged to exhibit temperature-responsive failure prior to the at least one thyristor as the
3 operating temperature of the memory device varies from a design operating temperature
4 thereof.

1 9 (original). The memory device of claim 8, wherein the reference thyristor is configured
2 and arranged to fail at a lower temperature than the at least one thyristor as the operating
3 temperature increases above the design operating temperature.

1 10 (original). The memory device of claim 8, wherein the reference thyristor is configured
2 and arranged to fail at a higher temperature than the at least one thyristor as the operating
3 temperature decreases below the design operating temperature.

1 11 (original). The memory device of claim 6, further comprising a plurality of memory cells,
2 each memory cell including a thyristor, wherein the first circuit further comprises:

3 a first reference memory cell including a thyristor and adapted to store a data "zero"
4 and to fail to retain the data "zero" as a function of the conductance state of the thyristor in the
5 first reference memory cell before other memory cells in the memory device fail data "zero";

6 a second reference memory cell including a thyristor and adapted to store a data "one"
7 and to fail to retain the data "one" as a function of the conductance state of the thyristor in the
8 second reference memory cell before other memory cells in the memory device fail data "one";
9 and

10 the second circuit being adapted to apply the second signal to the second control port as
11 a function of at least one of the first and second reference memory cells failing to retain data.

1 12 (original). The memory device of claim 11, wherein an emitter of the thyristor in the first
2 reference memory cell is coupled to a reference voltage signal that is greater than a reference
3 voltage signal coupled to at least one of the emitter regions of the thyristors in the plurality of
4 memory cells.

1 13 (original). The memory device of claim 11, wherein an emitter of the thyristor in the first
2 reference memory cell is coupled to a reference voltage signal that is less than a reference
3 voltage signal coupled to at least one of the emitter regions of the thyristors in the plurality of
4 memory cells.

1 14 (original). The memory device of claim 11, wherein each memory cell includes a pass
2 device coupled to an emitter region of the respective thyristor, each pass device exhibiting
3 leakage, the pass device in the second reference thyristor memory cell being adapted to leak
4 relatively more current than the pass devices in the plurality of memory cells such that the
5 second reference memory cell fails to retain data before the plurality of memory cells fail to
6 retain data.

1 15 (presently amended). The memory device of claim 6, wherein the second control port
2 and the second base region are configured and arranged such that the second signal increases
3 carrier depletion in the second base region ~~in the second base region~~.

1 16 (original). The memory device of claim 6, wherein the second control port extends over a
2 junction between the second base region and the second emitter region.

1 17 (original). The memory device of claim 16, wherein the second circuit is adapted to
2 capacitively couple the second signal to the second emitter region for accumulating carriers
3 therein.

1 18 (original). The memory device of claim 6, wherein the second control port extends over a
2 junction between the first and second base regions.

1 19 (presently amended). A semiconductor device comprising:
2 a thyristor having thyristor body regions including first and second immediately
3 adjacent base regions between first and second emitter regions, the thyristor body being
4 maintained in a conductance state as a function of holding current; and
5 a control circuit configured and arranged for applying a signal to at least one of the
6 base regions for controlling the holding current or forward blocking voltage as a function of
7 temperature, the signal being generated outside of the thyristor.

1 20 (original). The semiconductor device of claim 19, wherein the thyristor is a thin
2 capacitively-coupled thyristor.

1 21 (original). The memory device of claim 6, wherein the thyristor is a thin capacitively-
2 coupled thyristor.

1 22 (presently amended). The ~~memory~~ semiconductor device of claim 1, wherein the
2 thyristor is a thin capacitively-coupled thyristor.

1 23 (presently amended). The ~~memory~~ semiconductor device of claim 1, wherein one
2 of the base regions includes N-doped material having a higher concentration of N+
3 dopant in a depletion region that faces the second control port.

1 24 (presently amended). The ~~memory~~ semiconductor device of claim 1, wherein one
2 of the base regions includes material having defects in a depletion region facing the
3 second control port.

1 25 (original). The memory device of claim 6, wherein one of the base regions includes
2 N-doped material having a higher concentration of N+ dopant in a depletion region that
3 faces the second control port.

1 26 (original). The memory device of claim 6, wherein one of the base regions includes
2 material having defects in a depletion region facing the second control port.

1 27 (original). The semiconductor device of claim 19 further comprising a second control
2 port, wherein one of the base regions includes N-doped material having a higher
3 concentration of N+ dopant in a depletion region that faces the second control port.

1 28. (cancelled)